REMARKS

The claims are rejected in view of ALPERT (U.S. Patent 5,621,886) and a MIPS reference (MIPS64 5Kc™ Processor Core Datasheet). The independent claims are amended to more fully distinguish over the prior art of record. Reconsideration of the rejection in view of the foregoing amendments and the following remarks is respectfully requested.

Independent claim 1 is amended to recite the operation of "storing trace information in a trace memory". Support for this amendment may be found in paragraph [1021] and Figure 1, among other places.

Independent claim 1 is also amended to recite the operation of "applying trace regeneration software to said trace information to reconstruct said trace information after said task is executed on said processor". Support for this amendment may be found in paragraph [1022], among other places.

The foregoing amendments fully distinguish claim 1 over the prior art of record. The MIPS reference describes JTAG Debug Support, which is a dynamic or interactive operation performed by a user. For example, the MIPS reference states that "a debug exception is taken when a hardware breakpoint matches, whereby the normal application is suspended and debug mode is entered." The user then dynamically works in the debug mode.

Similarly, ALPERT discloses dynamic or interactive debug operations. For example, ALPERT states at column 5, lines 1-6: "This document describes an invention allowing for the separate enablement of debug events during the execution of operating system routines and non-operating system routines. This allows programmers the flexibility of selectively enabling debug events during the execution of either handlers, or applications, or both." ALPERT performs debug operations while a current process is suspended (see, for example, Figure 2).

The invention recited in claim 1 requires the "storing [of] trace information in a trace memory" and the further operation of "applying trace regeneration software to said trace information to reconstruct said trace information after said task is executed on said processor." MIPS and ALPERT fail to show or suggest such a technique since they are directed toward interactive debug operations. Accordingly, MIPS and ALPERT do not have the recited trace

memory and do not show or suggest trace regeneration software to reconstruct trace information. Further, MIPS and ALPERT in no way show or suggest the performance of such operations "after said task is executed on said processor." Rather, MIPS and ALPERT disclose an interactive process, not one that relies upon a trace memory and trace regeneration software to reconstruct trace information after a task is executed on the processor.

In the MIPS reference, "the normal application is suspended and debug mode is entered". Similarly, ALPERT suspends a current process. Thus, the prior art fails to show or suggest storing trace information in a trace memory and applying trace regeneration software to reconstruct the trace information after the task is executed, as claimed.

It is also important to note that MIPS and ALPERT do not initiate tracing in response to a combination of a processor mode and an ASID value, as claimed. The Examiner argues that MIPS teaches the ASID value and ALPERT teaches the processor mode. However, there is no identified teaching in either reference of the desirability of using both of these values in combination to initiate tracing. Moreover, the references individually rely upon these values to perform interactive debug operations, they do not show or suggest the use of a processor mode and an ASID value to store trace information in a trace memory and then use trace regeneration software to reconstruct trace information after a task is executed on the processor, as claimed.

In view of the foregoing amendments and remarks, it is respectfully submitted that amended claim 1 is now in a condition for allowance. Claims 3, 5-6, and 10 are dependent upon claim 1 and therefore should also be in a condition for allowance. Attention is particularly drawn to claim 10 which includes a number of limitations that are not shown or suggested by the prior art of record. The Examiner's rejection of this claim is completely inadequate as it fails to cite detailed teachings corresponding to the detailed elements of the claim.

The remaining independent claims are amended to include limitations of the type discussed in connection with claim 1. Thus, claims 11, 21, 22, and 24 should also be in a condition for allowance, as should dependent claims 13, 15-17, 20, and 23.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is now in condition for allowance. The Examiner is invited to contact the undersigned if there are any residual issues that can be resolved through a telephone call.

The Commissioner is hereby authorized to charge any appropriate fees to Deposit Account No. 03-3117.

Dated: June 3, 2005

Respectfully submitted,
COOLEY GODWARD LLP

By: _____
William S. Galliani
Reg. No. 33,885

Cooley Godward LLP
ATTN: Patent Group
Five Palo Alto Square
3000 El Camino Real
Palo Alto, CA 94306-2155
Tel: (650) 843-5000
Fax: (650) 857-0663